

FIG.1

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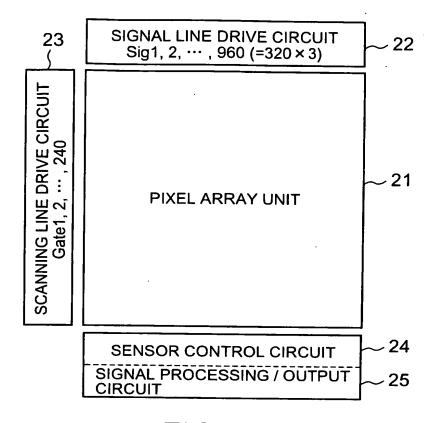


FIG.2

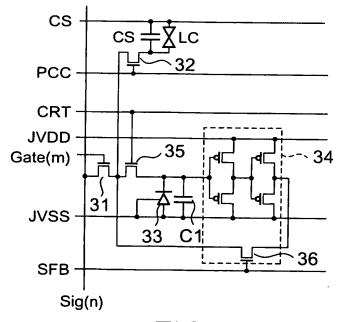


FIG.3

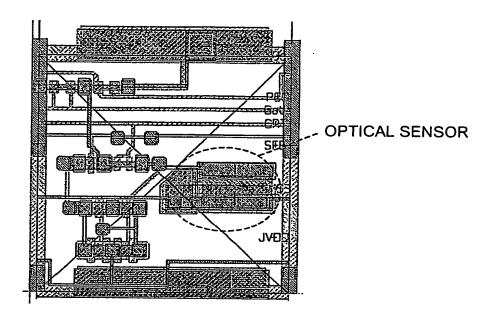


FIG.4

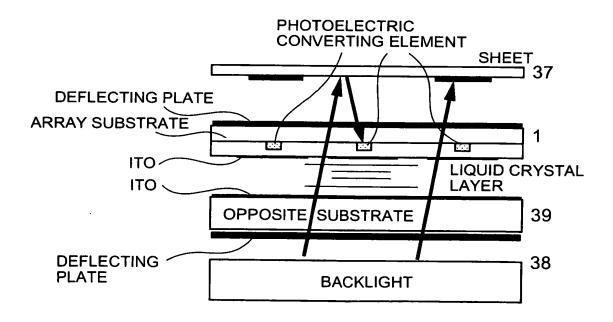
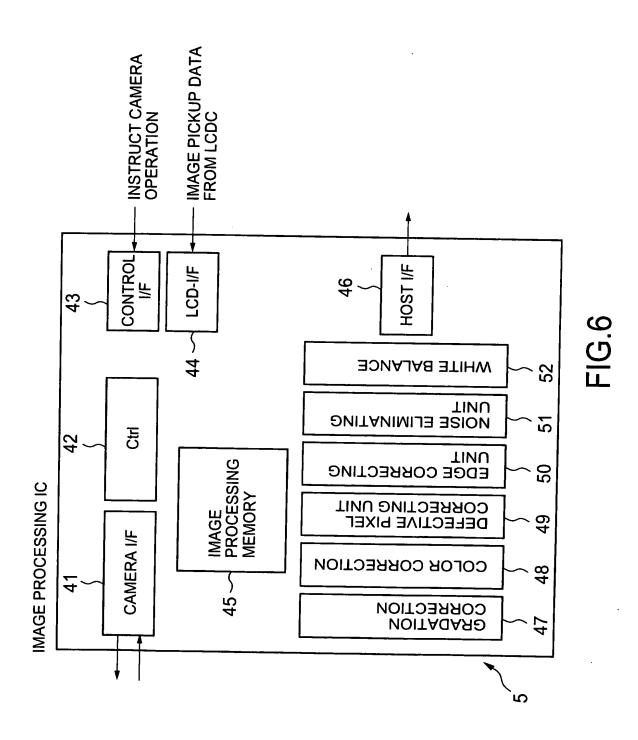


FIG.5





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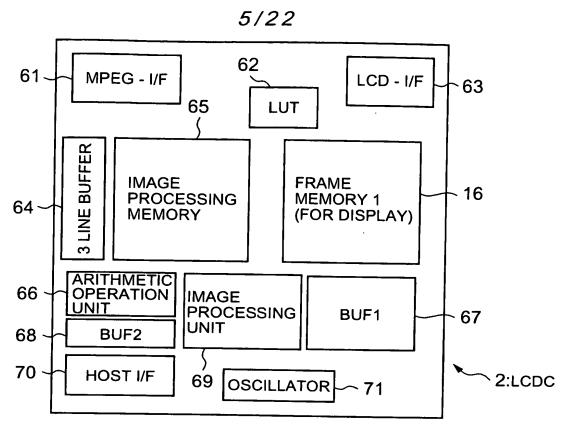


FIG.7

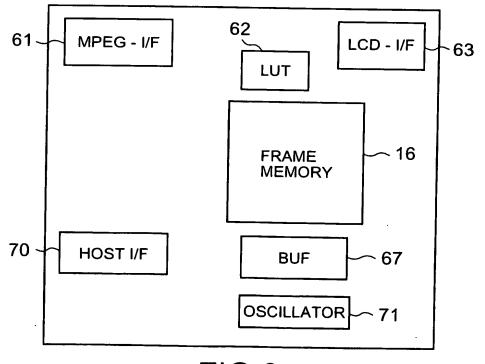
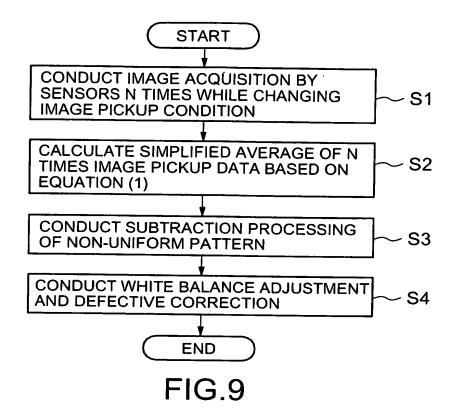


FIG.8

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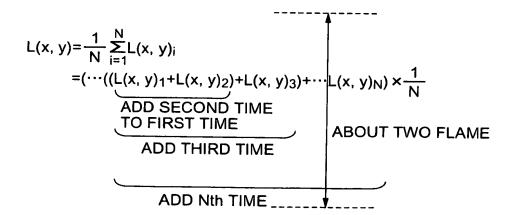


FIG.10

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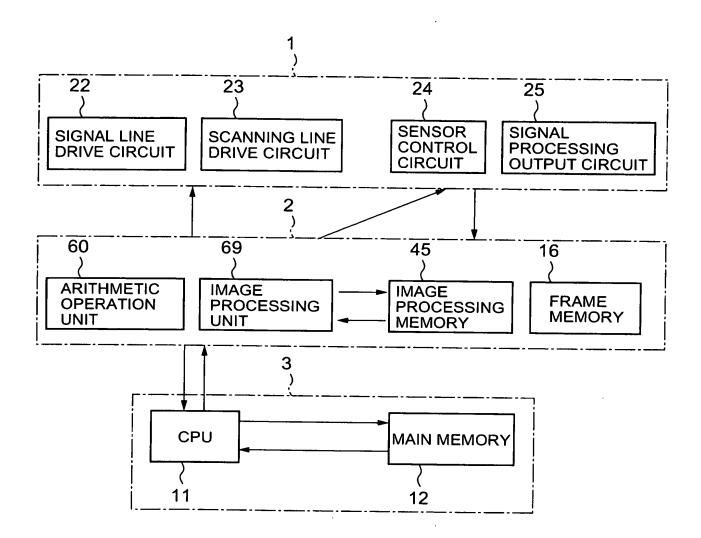


FIG.11

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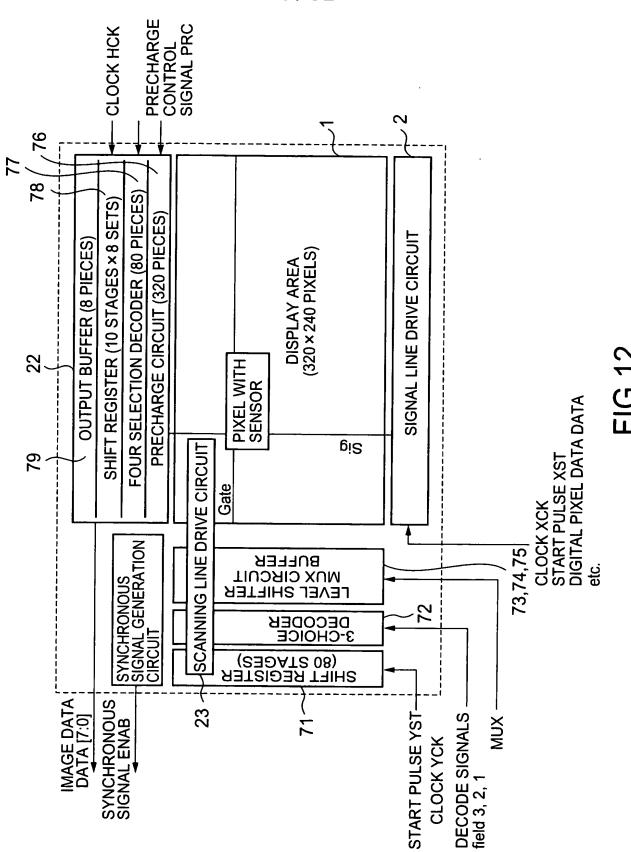


FIG. 12

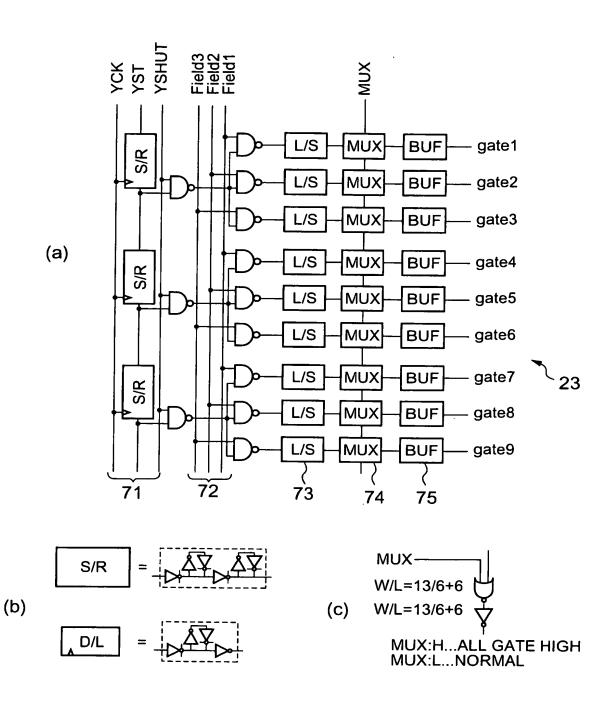
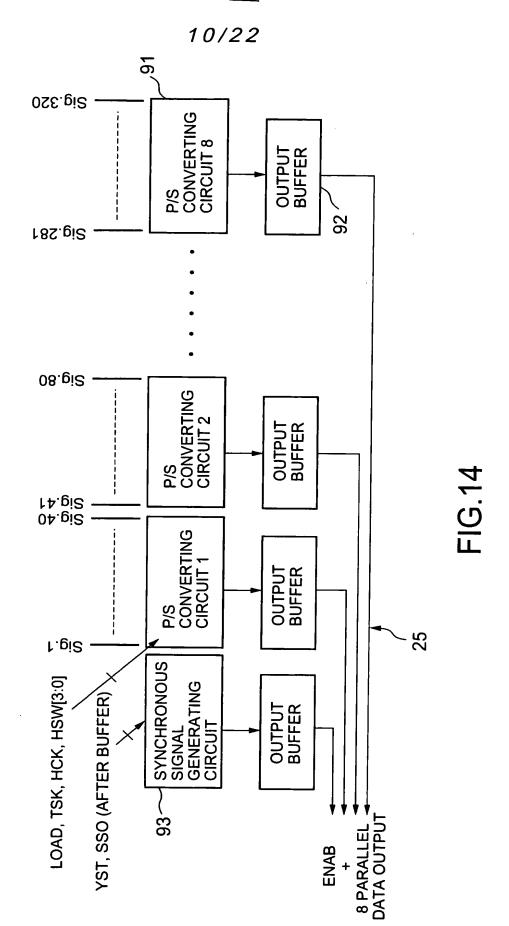


FIG.13



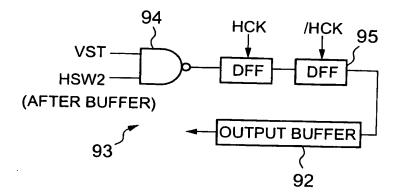


FIG.15

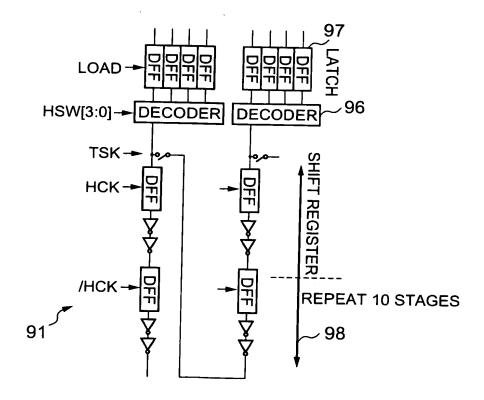


FIG.16

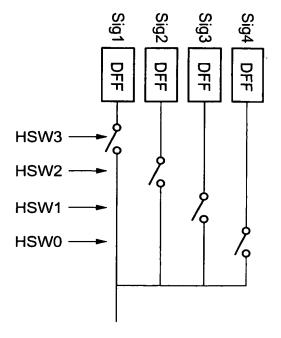


FIG.17

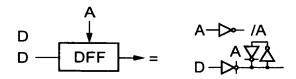


FIG.18

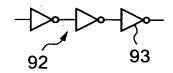


FIG.19

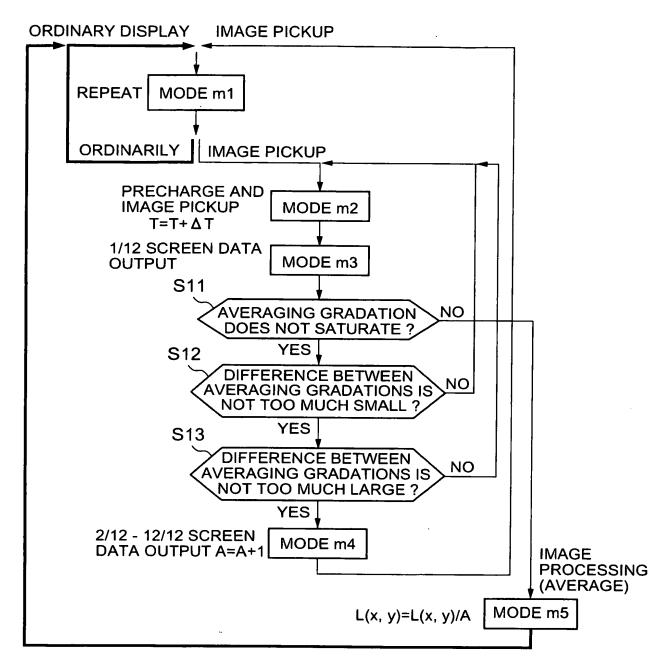
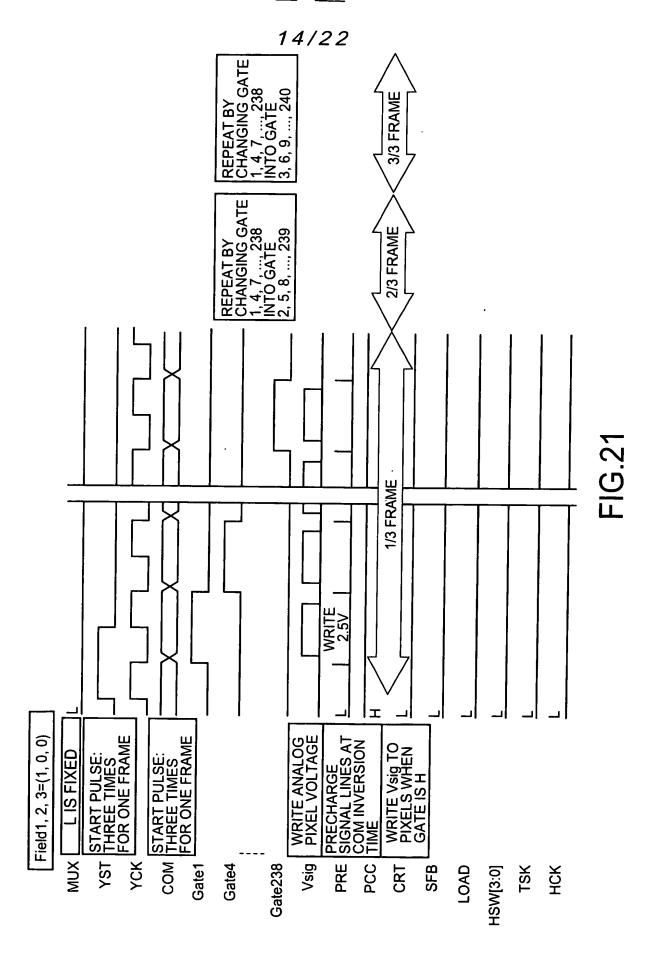


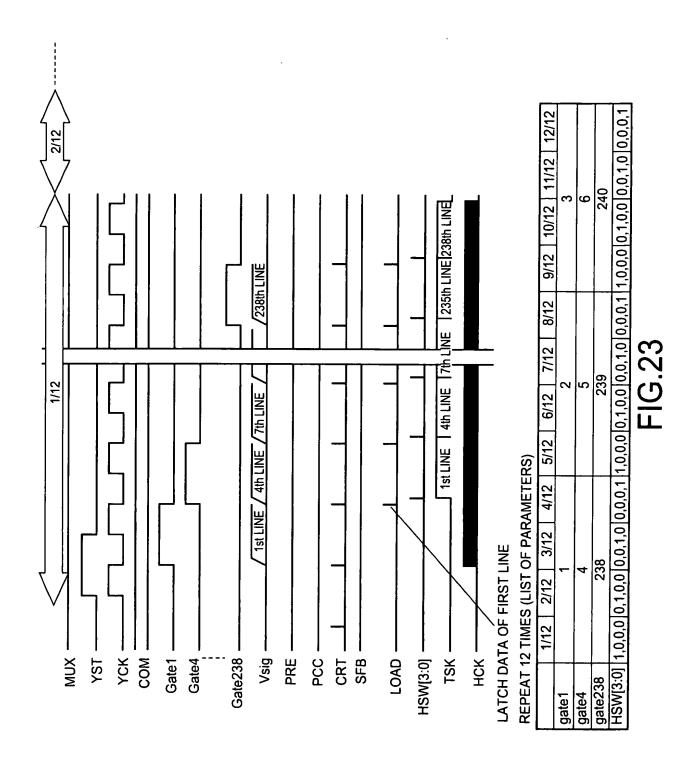
FIG.20



		COM IS FIXED	1	1
MUX	All ON @H		_	
YST			<u> </u>	
YCK				
СОМ	LISF	IXED OR H IS FIXED		
Gate1			_	
Gate2				
Gate240				
Vsig				
PRE	SENSOR CAPACITANCE	WRITE 5V		
PCC	IN PIXEL IS PRECHARGED	L		
CRT	REGUAROLD			
SFB			1	
LOAD		L		
HSW[3:0]		<u>L</u>		
TSK		L		
HCK		<u>L</u>		

FIG.22

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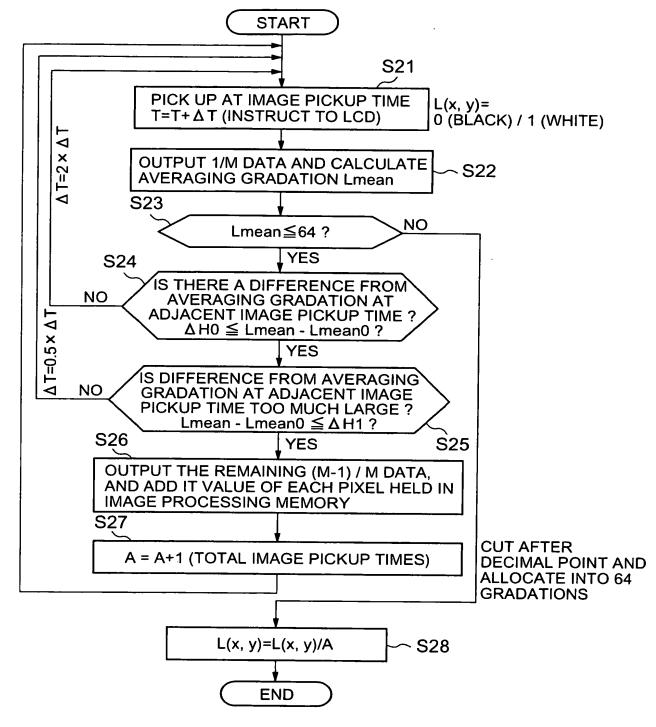


FIG.24

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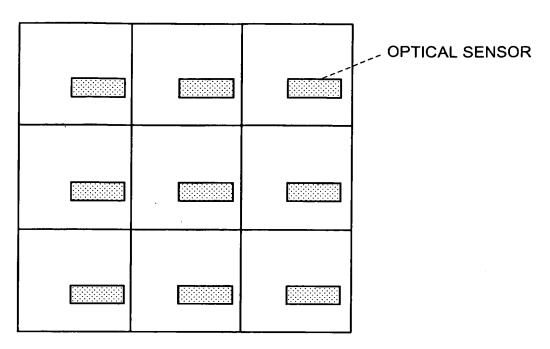


FIG.25

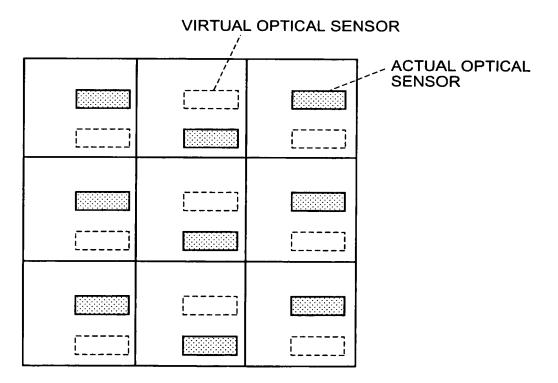


FIG.26

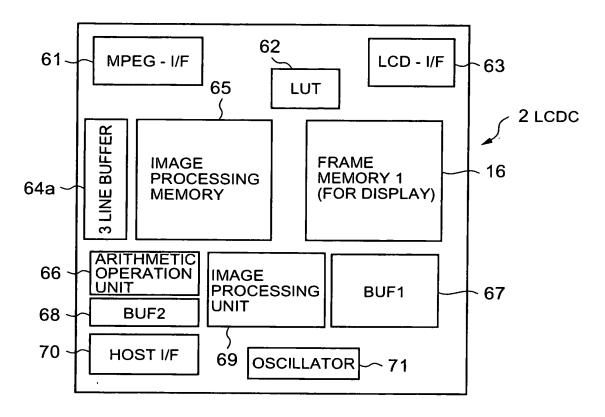


FIG.27

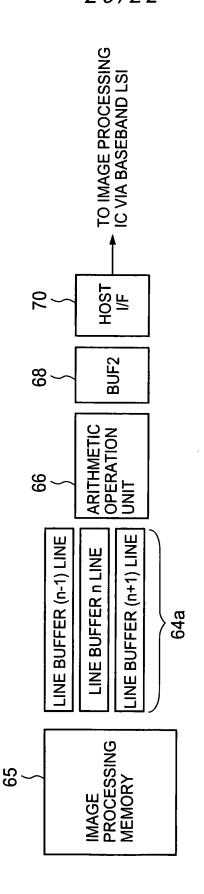


FIG.28

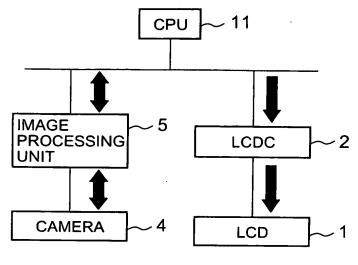


FIG.29

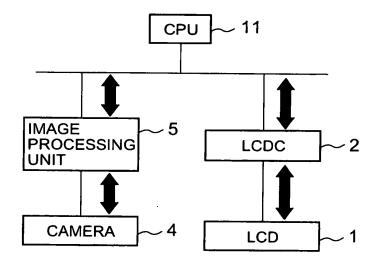


FIG.30

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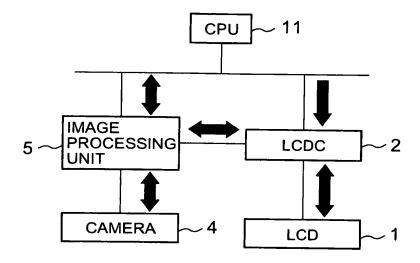


FIG.31